ATTACH #18

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
(Richmond Division)

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|---|---|
| RAMBUS INC.<br><br>Plaintiff,<br><br>v.<br><br>INFINEON TECHNOLOGIES AG, et al.,<br><br>Defendants. | Civil Action No. 3:00CV524 |

**DEFENDANT INFINEON TECHNOLOGIES AG 'S FIRST SUPPLEMENTAL RESPONSES TO PLAINTIFF'S INTERROGATORIES NOS. 3, 5 and 6**

Pursuant to Federal Rule of Civil Procedure 33, Plaintiff Infineon Technologies AG ("Infineon") hereby makes the following supplemental responses to Plaintiff Rambus, Inc.'s ("Rambus'") Interrogatories Nos. 3, 5 and 6. Each response herein is made subject to and without waiver of Infineon's previously-stated General and Specific Objections. Pursuant to Federal Rule of Civil Procedure 26(e), Infineon reserves the right to supplement its responses or document production if it learns of additional responsive information.

## SUPPLEMENTAL RESPONSES

INTERROGATORY NO. 3:

Identify each and every customer of Infineon that has purchased or is purchasing Infineon SDRAMs, DDR SDRAMs, or SGRAMs, or any modules that contain any such devices, within the United States or for inclusion in products sold or offered for sale in the United States, identifying the devices, modules or chip sets purchased and the date of purchase.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 3:

To the extent any consumers are identified in response to Interrogatory No. 3, Infineon responds pursuant to Fed. R. Civ. P. 33(d) that the answer to this interrogatory may be derived or ascertained from the business records of Infineon that have been produced in this action. Such documents include I 023284 - I 023309, I 089866 - I 08911 and I 141447 - I 141514.

INTERROGATORY NO. 5:

For each and every Infineon product or device accused of infringement in this action, identify on a claim chart (on a product-by-product basis) each limitation of each claim of the patents-in-suit that Infineon contends is not met by each such product or device, the basis for Infineon's contention that the limitation is not met literally or under the doctrine of equivalents, and all portions of the patents-in-suit and related prosecution file and/or prior art references that Infineon asserts support its contention.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 5:

Noninfringement of patent claims depends, in part, on the interpretation of claim language in the asserted claims. Claim construction is a question of law for the Court. In this case, the Court has not yet construed any claims of the patents-in-suit. Accordingly, Infineon reserves its rights to supplement or amend its responses to this interrogatory once the Court rules on the interpretation of the claim language in the asserted claims of the patents-in-suit. In addition, Rambus bears the burden of proof for infringement, but has not identified with specificity which of the accused products infringe each asserted claim. Accordingly, pursuant to Infineon's interpretation and

understanding of the asserted claims and Rambus' generic infringement contentions, the products accused by Rambus do not infringe for at least the following reasons:

A. **U.S. Patent No. 5,953,263**

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs, DDR SDRAMs and SGRAMs of literally infringing claims 1-5, 14-19, 21, 23-25, 27-28 and 30-33 of the '263 patent. Rambus does not, however, identify any specific circuitry or methods of operating a semiconductor memory device that allegedly infringe particular asserted claims. Infineon's investigation to date reveals that none of the accused products infringe the asserted claims of the '263 patent for one or more of the following reasons: 1) the accused products do not respond to read requests; 2) the accused products do not contain a programmable register to store a value that is representative of a delay time after which the memory device responds to a read request; 3) the accused products do not contain a programmable register to store a value that is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request; 4) the accused products do not include output drivers to output data onto an external bus after a number of clock cycles of an external clock transpire; 5) the accused products do not output data onto an external bus synchronously with respect to an external clock; 6) the accused products do not contain a programmable register to store a value representative of a number of clock cycles of a clock to transpire before data is output onto a bus in response to a read request; 7) the accused products do not include output drivers to output data onto a bus after a number of clock cycles of a clock transpire; 8) the accused products do not output data onto a bus synchronously with respect to a clock; 9) the accused products do not perform methods that include the steps of receiving and storing a time delay value in a programmable register that is representative of a number of clock cycles of an external clock to transpire before data is output onto an external

bus in response to a read request or a transaction request; and 10) the accused products do not perform methods that include the step of selecting one of a plurality of time delays after which the memory device provides data in response to a read request. In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted claims to cover the accused Infineon products, those claims are invalid over the prior art.

B. U.S. Patent No. 5,954,804

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs, DDR SDRAMs and SGRAMs of infringing claim 26 of the '804 patent. Rambus does not, however, identify any specific circuitry that allegedly infringes that particular claim. Infineon's investigation to date reveals that none of the accused products infringe the asserted claim of the '804 patent for one or more of the following reasons: 1) the accused products do not output data on an external bus synchronously with respect to first and second external clock signals; 2) the accused products do not respond to read requests, and do not contain an internal register to store a value which is representative of a number of clock cycles to transpire before responding to a read request; 3) the accused products do not contain delay locked loop circuitry to generate an internal clock signal using first and second external clock signals; 4) the accused products do not have interface circuitry, coupled to an external bus to receive a read request; and 5) the accused products do not output data on the external bus in response to an internal clock signal synchronously with respect to first and second external clock signals and in accordance with a value stored in a first internal register that is representative of a number of clock cycles to transpire before the device responds to a read request. In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted claim to cover the accused Infineon products, that claim is invalid over the prior art.

C. U.S. Patent No. 6,032,214

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs, DDR SDRAMs and SGRAMs of infringing claims 1, 2, 4, 6, 9-11, 14-16, 18, 19, 21, 24-26 and 29 of the '214 patent. Rambus does not, however, identify any specific circuitry or methods of operating a synchronous memory device that allegedly infringe particular claims. Infineon's investigation to date reveals that none of the accused products infringe the asserted claims of the '214 patent for one or more of the following reasons: 1) the accused Infineon products do not provide first block size information to a memory device in the form of a binary code or otherwise; 2) the accused Infineon products do not issue first or second read requests to a memory device; 3) the accused Infineon products do not have first and second external clock signals; 4) the accused devices do not output data on an external bus synchronously with respect to first and second external clock signals; 5) the accused products do not respond to read requests; 6) the accused products do not store a code in an access-time register that is representative of a number of clock cycles; and 7) and the accused Infineon products are not automatically precharged after executing a read request. In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted claims to cover the accused Infineon products, those claims are invalid over the prior art.

D. U.S. Patent No. 6,034,918

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs, DDR SDRAMs and SGRAMs of infringing claims 1, 2, 6, 8-9, 13, 15-20, 24, 25, 29-31, 33 and 34 of the '918 patent. Rambus does not, however, identify any specific circuitry or methods of operating and/or controlling a synchronous memory device that allegedly infringe particular asserted claims. Infineon's investigation to date reveals that none of the accused products infringe the asserted claims of the '918 patent for one or more of the following reasons: 1) the accused products do not provide

first or second block size information to a memory device, wherein the block size information defines an amount of data; 2) the accused products do not issue first or second read requests to a memory device; 3) the accused products do not issue first or second write requests to a memory device; 4) the accused products do not output data corresponding to first or second block size information onto the bus synchronously with respect to an external clock signal; 5) the accused products do not provide or store a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request; 6) the accused products do not receive first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request; 7) the accused products do not output a first amount of data corresponding to first block size information, in response to a first read request, onto a bus synchronously with respect to an external clock signal; 8) the accused products do not output a first amount of data corresponding to first block size information in response to a second read request onto a bus synchronously with respect to an external clock signal; 9) the accused products do not input a first amount of data corresponding to first block size information in response to a first write request, from a bus synchronously with respect to an external clock signal; 10) the accused products do not store a value in a time delay register, the value being representative of a number of external clock cycles to transpire; 11) the accused products do not receive block size information from a bus controller wherein the block size information defines a first amount of data to be output by the memory device onto the bus in response to a read request; 12) the accused products do not output a first amount of data corresponding to block size information in response to a first read request; 13) the accused products do not output data synchronously with respect to an external clock signal during a plurality of clock cycles of an external clock signal in accordance with a value stored in a time delay register; and 14) the accused Infineon

products do not use a DLL to generate an internal clock signal. In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted claims to cover the accused Infineon products, those claims are invalid over the prior art.

INTERROGATORY NO. 6:

If Infineon contends that any or all of the claims of the patents-in-suit are invalid or unenforceable, state the basis for such contention by identifying each such patent and claim, each fact underlying such contention, including the identification of any alleged prior act, the individuals who have knowledge of the facts underlying such contention, and all documents related to such contention.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 6:

Based on its investigation to date, each of the asserted claims of the patents-in-suit are invalid and/or unenforceable for one or more of the following reasons:

The patents-in-suit are unenforceable due to patent misuse and estoppel due to Rambus' misconduct at JEDEC because throughout its tenure as a JEDEC member, under the policies and rules of JEDEC, Rambus was obligated to disclose any patents or patent applications that might be involved in the work of any of the committee meetings that its representatives attended. As of 1992, Rambus believed that its pending patent applications covered the SDRAM technology being discussed for standardization by JEDEC Committee 42.3. Further, pursuant to its patent strategy, at various times during its tenure as a member of JEDEC, Rambus filed continuation patent applications for the express purpose of filing claims to track the SDRAM technology being discussed at the JEDEC meetings its representatives attended. Rambus attended no less than 15 JEDEC committee 42.3 meetings during which SDRAM standardization was discussed, but never disclosed to the JEDEC members that it had pending patent applications that it believed covered the work being discussed by the committee nor did it disclose that it intended

and did file claims to cover the work of the committee. Instead, the only disclosures of intellectual property rights by Rambus were patents that did not relate to the work being done by the committee. In reliance of Rambus' silence with regard to patents and patent applications that might relate to the SDRAM standardization work, JEDEC and its members, including Infineon, unknowingly adopted SDRAM standards that Rambus now claims are covered by its patents. Further Infineon has made substantial investments in developing, manufacturing and selling SDRAM and DDR SDRAM products that are compatible with the JEDEC standards, believing these standards to be open standards. The details of the factual basis for Infineon's affirmative defense that the patents-in-suit are unenforceable due to equitable estoppel and patent misuse are set forth in paragraphs 74-194 of Infineon's Answer and Counterclaims to Rambus' First Amended Complaint, which are incorporated by reference in their entirety in this response. Moreover, Rambus' delay in filing the patent applications that contain the asserted claims until after it terminated its membership in JEDEC constitutes laches.

A. **U.S. Patent No. 5,953,263**

The '263 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '263 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '263 patent, including patent applications through which the '263 patent claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1. U.S. Patent No. 5,140,688; and

2. Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596 (collectively "SCI publications"), including:

a. David B. Gustavson et al.," The Scalable Coherent Interface Project (Superbus)", draft of August 22,1988;

b. David B. Gustavson, "Scalable Coherent Interface", November 1988, (paper to appear at COMPCON Spring 1989);

c. David V. James, "Scalable I/O Architecture for Buses", November 1988, (paper to appear at COMPCON Spring 1989);

d. David V. James, "P1596: SCI, A Scalable Coherent Interface", November 1988, (transparencies);

e. Knut Alnes, "SCI: A Proposal For SCI Operation", November1988;

f. Knut Alnes, "SCI: A Proposal For SCI Operation", January 1989;

g. Bjørn O. Bakka et al., "SCI: Logical Level Proposals", January 1989;

h. Ernst H. Kristiansen et al., "Scalable Coherent Interface", February 1989, (paper to appear in Eurobus Conference Proceedings, Munich, May 1989);

i. Morten Schanke, "Proposal For Clock Distribution in SCI", May 1989; and

j. Ernst H. Kristiansen et al., "Scalable Coherent Interface", Eurobus, London, September1989.

Claims 1, 18, 24-25 and 27 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. U.S. Patent No. 3,950,735;

2. Japanese Patent Application 54-160587;

3. U.S. Patent No. 4,445,204;

4. Japanese Patent Application 55-89232;

5. Japanese Patent Application 58-186919;

6. U.S. Patent No. 4,858,113;

7. U.S. Patent No. 4,953,128;

8. U.S. Patent No. 5,140,688;

9. Japanese Patent Application 62-51509;

10. Japanese Patent Application 62-71428;

11. Japanese Patent Application 62-185253;

12. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens; and

13. Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

Claims 2-3, 14-15 and 30-31 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. U.S. Patent No. 3,950,735;

2. Japanese Patent Application 54-160587;

3. U.S. Patent No. 4,445,204;

4. Japanese Patent Application 55-89232;

5. Japanese Patent Application 58-186919;

6. U.S. Patent No. 4,858,113;

7. U.S. Patent No. 4,953,128;

8. U.S. Patent No. 5,140,688;

9. Japanese Patent Application 62-71428;

10. Japanese Patent Application 62-185253;

11. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens; and

12. Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

Claims 4 and 23 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 54-160587;
2. U.S. Patent No. 4,445,204;
3. Japanese Patent Application 55-89232;
4. Japanese Patent Application 58-186919;
5. U.S. Patent No. 4,858,113;
6. U.S. Patent No. 4,953,128;
7. U.S. Patent No. 5,140,688;
8. Japanese Patent Application 62-51509;
9. Japanese Patent Application 62-71428;
10. Japanese Patent Application 62-185253; and
11. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 5, 19, 21 and 28 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 54-160587;
2. Japanese Patent Application 55-89232;
3. Japanese Patent Application 58-186919;
4. U.S. Patent No. 4,858,113;
5. U.S. Patent No. 4,953,128;
6. U.S. Patent No. 5,140,688;

7. Japanese Patent Application 62-51509;

8. Japanese Patent Application 62-71428; and

9. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 16 and 32 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 54-160587;

2. U.S. Patent No. 4,445,204;

3. Japanese Patent Application 55-89232;

4. Japanese Patent Application 58-186919;

5. U.S. Patent No. 4,858,113;

6. U.S. Patent No. 4,953,128;

7. U.S. Patent No. 5,140,688;

8. Japanese Patent Application 62-71428;

9. Japanese Patent Application 62-185253; and

10. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 17 and 33 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 54-160587;

2. Japanese Patent Application 55-89232;

3. Japanese Patent Application 58-186919;

4. U.S. Patent No. 4,858,113;

5. U.S. Patent No. 4,953,128;

6. U.S. Patent No. 5,140,688;

7. Japanese Patent Application 62-71428; and

8. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

The asserted claims of the '263 patent are also invalid under 35 U.S.C. § 112 for omitting elements that one of ordinary skill in the art would understand as being essential to the alleged invention as originally disclosed, and for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "transaction request," "to output data on the bus, in response to the read request, synchronously with respect to an external clock," "the value is representative of a number of clock cycles of the external clock," "a programmable register to store a value which is representative of a number of clock cycles of an external clock," "wherein the output drivers output data on the bus after the number of clock cycles of the external clock transpire," "wherein the value is representative of a fraction or a whole number of clock cycles of the external clock" and "receiving a time delay value, wherein the delay value is representative of a number of clock cycles of an external clock."

**B. U.S. Patent No. 5,954,804**

The '804 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '804 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '804 patent, including patent applications through which the '804 patent

claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1. U.S. Patent No. 4,998,262; and

2. Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596, including the publications listed in Section A as 2(a)-(j).

Claim 26 of the '804 patent is invalid under 35 U.S.C. § 102 and/or § 103, in view of the above references and the references listed below, either alone or in combination with each other and/or the general knowledge of one of skill in the art:

1. U.S. Patent No. 3,950,735;

2. Japanese Patent Application 54-160587;

3. U.S. Patent No. 4,445,204;

4. Japanese Patent Application 55-89232;

5. Japanese Patent Application 58-186919;

6. U.S. Patent No. 4,858,113;

7. U.S. Patent No. 4,953,128;

8. U.S. Patent No. 5,140,688;

9. Japanese Patent Application 62-51509;

10. Japanese Patent Application 62-71428;

11. Japanese Patent Application 62-185253;

12. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens;

13. Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

14. U.S. Patent No. 4,338,569; and

15. U.S. Patent No. 5,361,277.

Claim 26 of the '804 patent is also invalid under 35 U.S.C. § 112 for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "first and second external clock signals," "interface circuitry, coupled to the external bus to receive a read request" and "outputs data on an external bus synchronously with respect to first and second external clock signals."

C. U.S. Patent No. 6,032,214

The '214 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '214 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '214 patent, including patent applications through which the '214 patent claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1. U.S. Patent No. 3,771,145; and

2. Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596, including the publications listed in Section A as 2(a)-(j).

The asserted claims of the '214 patent are invalid under 35 U.S.C. § 102 and/or § 103, in view of the above references and the references listed below, either alone or in combination with each other and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 63-239676;

2. U.S. Patent No. 4,763,249;

3. Unisys JEDEC Presentation - December 6, 1988;

4. Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate*, 1990 IEEE International Solid-State Circuits Conference, pp. 232-33, 303, February 16, 1990;

5. Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate and On-Chip ECC*, 1990 IEEE Journal of Solid-State Circuits, vol. 25, no. 5, pp. 1118-28, October 1990;

6. Japanese Patent Application 63-142445;

7. *Fast Packet Bus for Microprocessor Systems with Caches*, IBM Technical Disclosure Bulletin, vol. 31, no. 8, pp. 279-82, January 1989;

8. Watanabe, *High-Density SRAMs*, 1987 IEEE International Solid-State Circuits Conference, pp. 266-67; February 27, 1987;

9. Japanese Patent Application 61-72350;

10. U.S. Patent No. 5,134,699;

11. U.S. Patent No. 4,315,308

12. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens;

13. Anceau, *A Synchronous Approach for Clocking VLSI Systems*, IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 1, February 1982;

14. German Laid-Open Patent Application DE 3733554 A1, published April 21, 1988;

15. Motorola's MC88200 chip;

16. Ogiue et al., *13-ns, 500-mW, 64-kbit ECL RAM Using HI-BICMOS Technology*, IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986;

17. U.S. Patent No. 4,205,500;

18. U.S. Patent No. 4,803,621;

19. U.S. Patent No. 4,870,622;

20. U.S. Patent No. 4,926,385;

21. U.S. Patent No. 4,927,791;

22. U.S. Patent No. 4,480,307;

23. U.S Patent No. 5,179,667;

24. U.S. Patent No. 4,773,066;

25. U.S. Patent No. 4,851,990;

26. U.S. Patent No. 4,878,166

27. U.S. Patent No. 4,528,661;

28. U.S. Patent No. 4,849,965;

29. U.S. Patent No. 4,435,762;

30. U.S. Patent No. 4,949,301;

31. U.S. Patent No. 4,835,674;

32. U.S. Patent No. 4,839,801;

33. U.S. Patent No. 4,589,108;

34. U.S. Patent No. 5,029,124;

35. U.S. Patent No. 4,625,307;

36. U.S. Patent No. 4,748,617;

37. U.S. Patent No. 5,193,193;

38. U.S. Patent No. 4,482,999;

39. U.S. Patent No. 4,566,099;

40. U.S. Patent No. 4,047,246;

41. U.S. Patent No. 4,048,673;

42. U.S. Patent No. 4,519,034;

43. Voelker, IEEE Spectrum, Feb. 1987;

44. Dix et al, IBM Journal of Research and Development Vol 26, #4 July 1982;

45. Grossman, IBM Systems Journal, Vol. 24, No. S3/4 1985; and

46. U.S. Patent No. 3,950,735.

The asserted claims of the '214 patent are also invalid under 35 U.S.C. § 112 for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "write request," outputting data "synchronously with respect to a first and second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal," and "storing a code in an access-time register, the code being representative of a number of clock cycles of the first and second external clock signals to transpire before data is output."

D. **U.S. Patent No. 6,034,918**

The '918 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '918 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '918 patent, including patent applications through which the '918 patent claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1. U.S. Patent No. 3,771,145; and

2. Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596, including the publications listed in Section A as 2(a)-(j).

The asserted claims of the '918 patent are invalid under 35 U.S.C. § 102 and/or § 103, in view of the above references and the references listed below, either alone or in combination with each other and/or the general knowledge of one of skill in the art:

1. Japanese Patent Application 63-239676;

2. U.S. Patent No. 4,763,249;

3. Unisys JEDEC Presentation - December 6, 1988;

4. Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate*, 1990 IEEE International Solid-State Circuits Conference, pp. 232-33, 303, February 16, 1990;

5. Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate and On-Chip ECC*, 1990 IEEE Journal of Solid-State Circuits, vol. 25, no. 5, pp. 1118-28, October 1990;

6. Japanese Patent Application 63-142445;

7. *Fast Packet Bus for Microprocessor Systems with Caches*, IBM Technical Disclosure Bulletin, vol. 31, no. 8, pp. 279-82, January 1989;

8. Watanabe, *High-Density SRAMs*, 1987 IEEE International Solid-State Circuits Conference, pp. 266-67; February 27, 1987;

9. Japanese Patent Application 61-72350;

10. U.S. Patent No. 5,134,699;

11. U.S. Patent No. 4,315,308

12. ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens;

13. Anceau, *A Synchronous Approach for Clocking VLSI Systems*, IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 1, February 1982;

14. German Laid-Open Patent Application DE 3733554 A1, published April 21, 1988;

15. Motorola's MC88200 chip;

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28. U.S. Patent No. 4,849,965;

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33. U.S. Patent No. 4,589,108;

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46. U.S. Patent No. 3,950,735.

The asserted claims of the '918 patent are also invalid under 35 U.S.C. § 112 for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "write request," "providing first block size information to the memory device, wherein the first block size information defines a first amount of data," "issuing a first read request," "outputs the first amount of data corresponding the first block size information synchronously with respect to an external clock signal," "issuing a second read request," "providing a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request," "receiving the external clock signal wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time," "wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles," "receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output," "in response to a read request," "outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal," "receiving a second read request," "outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the external clock signal," "receiving a first write request," and "inputting the amount of data corresponding to the second block size information, in response to the second write request, from the bus synchronously with respect to the external clock signal."